What is claimed is:

1. A resistance calibration circuit in a semiconductor device comprising:

a correction code generating means for generating a plurality of push-up code signals and a plurality of pull-down code signals based on an external reference resistor, wherein a reference voltage is applied to the correction code generating means;

a push-up decoder for decoding the plurality of push-up code signals from the correction code generating means;

a pull-down decoder for decoding the plurality of pull-down code signals from the correction code generating means; and

a resistance adjustor for receiving a push-up signal from the push-up decoder and a pull-down signal from the pull-down decoder and for turning on/off a plurality of inner transistors.

2. The resistance calibration circuit in accordance with claim 1, wherein the correction code generating means includes:

a first OP amplifier for comparing a voltage applied to the external reference resistor with a reference voltage applied to a second input terminal, outputting a first logic level if the voltage applied to the first input terminal is higher than the reference voltage, and outputting a second

logic level if the voltage applied to the first input terminal is lower than the reference voltage;

a first calculating means for producing the push-up code signals using an input signal from the first OP amplifier;

a first PMOS transistor group having a plurality of PMOS transistors, each of which has a gate to receive the push-up code signals and a source connected to a power supplier;

a first resistor connected to drains of the first PMOS transistor group and the first input terminal of the first OP amplifier;

a second PMOS transistor group having a plurality of PMOS transistors, each of which has a gate to receive the push-up code signals and a source connected to the power supplier;

a second resistor connected to drains of the second PMOS transistor group;

a second OP amplifier connected to the second resistor, wherein the second OP amplifier compares a voltage applied to a first input terminal with the reference voltage applied to a second input terminal, outputs the first logic level if the voltage applied to the first input terminal is higher than the reference voltage and outputs the second logic level if the voltage applied to the first input terminal is lower than the reference voltage;

a second calculating means for producing the pull-down code signals using an input signal from the second OP amplifier;

a first NMOS transistor group having a plurality of NMOS transistors, each of which has a gate to receive the pull-down code signals and a source connected to the power supplier;

a third resistor connected to drains of the first NMOS transistor group and a first input terminal of the second OP amplifier; and

a controller for controlling the first and second means.

3. The resistance calibration circuit in accordance with claim 2, wherein the push-up decoder includes:

a first NAND gate for NANDing first and second enable signals;

a first NOR gate for NORing a first push-up code signal and an output signal from the first NAND gate;

a second NOR gate for NORing a second push-up code signal and the output signal from the first NAND gate;

a third NOR gate for NORing a third push-up code signal and the output signal from the first NAND gate;

a fourth NOR gate for NORing output signals from the first and second NOR gates;

a first inverter for inverting an output signal from the first NOR gate;

a second inverter for inverting an output signal from the second NOR gate;

a third inverter for inverting an output signal from the third NOR gate;

a second NAND gate for NANDing output signals from the first and second NOR gates;

a fifth NOR gate for NORing output signals from the first to third inverters and outputting a first bit of the push-up signal;

a sixth NOR gate for NORing output signals from the second and third inverters and outputting a second bit of the push-up signal;

a seventh NOR gate for NORing an output signal from the fourth NOR gate and an output signal from the third inverter and outputting a third bit of the push-up signal, wherein the third NOR gate outputs a fourth bit of the push-up signal by NORing a third push-up code signal and the output signal from the first NAND gate;

a third NAND gate for NANDing an output signal from the second NAND gate and the output signal from the third inverter and outputting a fifth bit of the push-up signal;

a fourth NAND gate for NANDing output signals from the second and third inverters and outputting a sixth bit of the push-up signal;

a fifth NAND gate for NANDing output signals from the first to third inverters and outputting a seventh bit of the push-up signal; and

a fourth inverter for inverting an output signal from the first NAND gate and outputting an eighth bit of the push-up signal.

4. The resistance calibration circuit in accordance with claim 3, wherein the pull-down decoder includes:

a sixth NAND gate for NANDing the first and second enable signals;

an eight NOR gate for NORing a first pull-down code signal and an output signal from the sixth NAND gate;

a ninth NOR gate for NORing a second pull-down code signal and the output signal from the sixth NAND gate;

a tenth NOR gate for NORing a third push-up code signal and the output signal from the sixth NAND gate;

a fifth inverter for inverting an output signal from the eight NOR gate;

a sixth inverter for inverting an output signal from the ninth NOR gate;

a seventh inverter for inverting an output signal from the tenth NOR gate;

a seventh NAND gate for NANDing output signals from the fifth and sixth inverters;

an eight inverter for inverting an output signal from the fifth inverter;

a ninth inverter for inverting an output signal from the sixth inverter;

a tenth inverter for inverting an output signal from the seventh inverter;

an eleventh NOR gate for NORing output signals from the fifth and sixth inverters;

an eight NAND gate for NANDing output signals from the eight to tenth inverters and outputting a first bit of the pull-down signal;

a ninth NAND gate for NANDing output signals from the ninth and tenth and tenth inverters and outputting a second bit of the pull-down signal;

a tenth NAND gate for NANDing output signals from the seventh NAND gate and the tenth inverter and outputting a third bit of the pull-down signal, wherein the seventh inverter outputs a fourth bit of the pull-down signal by inverting an output signal from the tenth NOR gate;

a twelfth NOR gate for NORing output signals from the eleventh NOR gate and the tenth inverter and outputting a fifth bit of the pull-down signal;

a thirteenth NOR gate for NORing output signals from the ninth to tenth inverters and outputting a sixth bit of the pull-down signal; and

a fourteenth NOR gate for NORing output signals from the eight to tenth inverters and outputting a seventh bit of the pull-down signal, wherein the sixth DAND gate outputs an eighth bit of the pull-down signal by NANDing the first and second enable signals.

5. The resistance calibration circuit in accordance with claim 4, wherein the resistance adjustor includes:

a third PMOS transistor group having a plurality of PMOS transistors, each of which has a gate to receive the push-up signal, a source connected to the power supplier;

a fourth resistor connected to drains of the third PMOS transistor group and an I/O terminal thereof;

a second NMOS transistor group having a plurality of NMOS transistors, each of which has a gate to receive the pull-down signal, a source connected to a ground voltage level; and

a fifth resistor connected to drains of the second NMOS transistor group and the I/O terminal thereof.

6. A resistance calibration circuit in a semiconductor device, wherein the resistance calibration circuit is coupled to an I/O terminal of the semiconductor device, the resistance calibration circuit comprising;

a first resistor connected to the I/O terminal;

a second resistor connected to the I/O terminal;

a plurality of push-up transistors connected to the first resistor and controlled by a push-up signal, wherein the push-up transistors are in parallel connected to each other;

a plurality of pull-down transistors connected to the second resistor and controlled by a pull-down signal, wherein the pull-down transistors are in parallel connected to each other; and

a control signal generator for producing the push-up signal and the pull-down signal based on a voltage variation

of a voltage difference between a reference voltage and an external voltage, wherein the external voltage is applied to a fixed resistor.

7. The resistance calibration circuit in accordance with claim 6, wherein the control signal generator includes:

a correction code generating means for generating a plurality of push-up code signals and a plurality of pull-down code signals based on an external reference resistor, wherein a reference voltage is applied to the correction code generating means;

a push-up decoder for decoding the plurality of push-up code signals from the correction code generating means;

a pull-down decoder for decoding the plurality of pull-down code signals from the correction code generating means; and

a resistance adjustor for receiving a push-up signal from the push-up decoder and a pull-down signal from the pull-down decoder and for turning on/off a plurality of inner transistors.